REMARKS

Claims 1-42 are pending in the application.

Claims 1-5, 9-27, 29-32, 37, 38, 41 and 42 have been rejected.

Claims 6-8, 28, 33-36, 39-40 have been objected to.

Reconsideration of the Claims is respectfully requested.

1. Rejection under 35 U.S.C. § 103

Claim 1-5, 9, 11, 12, 14-18, 22, 24, 27, 29-32, 38, and 41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,657,953 to Hiramoto et al. ("Hiramoto") in view of U.S. Patent No. 4,667,324 to Graves ("Graves").

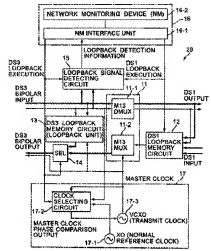
Claims 13 and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hiramoto in view of Graves as applied to claim 1 above, and further in. view of U.S. Patent No. 4,360,912 to Metz et al. ("Metz").

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142, p. 2100-125 (Rev. 5, August 2006) (citations omitted).

Hiramoto relates to providing "a signal loopback device which can ensure protection against a malfunction in consideration of erroneous signal detection due to degradation in circuit quality, can independently detect for each channel a loopback execution/cancellation signal sent for each channel by common hardware, and can also detect a failure of a remote station, thereby clearing a loopback control state prior to the failure." (Hiramoto 1:66-67, 2:1-7). Hiramoto illustrates its

"signal loopback device 20 . . . built in the multiplexing/demultiplexing devices (53, 63) and includes . . . a clock generating circuit 17:"

FIG.2



(Hiramoto 5:53-59). Hiramoto recites that the mux/demux 11 is for signal formats with differing rates, in that a "multiplexing/demultiplexing unit 11 carries out multiplexing/demultiplexing between a DS3 signal serving as a digital signal conforming to a [Digital Signal 3] C-bit parity system and a [Digital Signal 1, or T1] signal serving as a digital signal having a lower speed than that of the DS3 signal." (Hiramoto 4:1-5).

With regard to the clock circuitry, Hiramoto recites that the clock generating unit 17 "generates a read clock for the DS3 signal loopback memory circuit 13 and an operation clock of the M13 MUX 11-2 serving as the multiplexing unit." (Hiramoto 12:64-67). The "clock selecting circuit 17-2 includes a selector circuit 17-2-1 . . . [that] selects any one of a receive clock and a transmit (master) clock depending upon the signal from the [network monitoring" interface unit 16-1." (Hiramoto 13:7-14).

As noted in the Final Office Action at page 3, Hiramoto does not refer to a multistage bit stream multiplexer. Applicant further respectfully submits that Hiramoto does not refer to a bitstream multiplexer having a switchable forward/reverse clock relationship as recited in Applicant's claimed invention.

Graves teaches away from multistage multiplexers - it relates to "standard tributaries, . . . , either synchronous or asynchronous, at different order bit rates, can be multiplexed or

demultiplexed in a *single stage network* thus *eliminating the necessity for intermediate stages*." (Graves 2:58-63 (emphasis added)).

In its teaching *against intermediate stages for multiplexer and/or demultiplexers*, Graves notes that additional complex tributary structures are interspersed with synchronization bit stuffing devices, which inject synchronization bits into the tributaries according to the applicable stage of a digital signal standards specification. Graves, *in its teaching against multiple stage multiplexers and/or demultiplexers*, depicts in its Figure 1 a "multiplexed digital transmission system:"

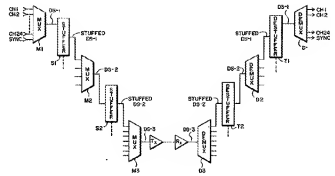


FIG. 1 PRIOR ART

That is, Graves recites that these *additional complex tributary systems* receive "PCM signals from twenty-four 64 kb/s channels CH1, CH2-CH24, [that] are multiplexed in a multiplexer M1 together with a synchronization bit to form a DS-1 bit stream at its output. Up to four such tributaries are bit stuffed in a stuffer S1 and then multiplexed in a multiplexer M2 together with further control bits to produce a DS-2 bit stream at its output. Seven such tributaries are then further bit stuffed in a stuffer S3 and multiplexed in a multiplexer M3 together with still further control bits to produce a DS-3 bit stream." (Graves 2:1-10; *see* Graves Figure 1).

Further, as Graves teaches against multi-stage multiplexers/demultiplexers, Graves also does not refer to a multistage bit stream multiplexer having a switchable forward/reverse clock relationship.

Metz relates to a "modular bus system for monitoring the status of a plurality of geographically distributed data points." (Metz 1:30-37). Metz was cited in rejection to Applicant's claims 13 and 26 in that the "[reconfigurable bus] system's single point transmitters, as well as the multiplexed transmitters, are fabricated from low power, complementary metal-

oxide semiconductor (CMOS) parts which enables each transmitter 8 to operate without a separate power supply." (Metz 6:11-16). Metz, however, does not refer to a multistage bit stream multiplexer having a switchable forward/reverse clock relationship.

As distinguished from the cited references, Applicant's Specification at page 19 explains that "inputs at multiplexer 330 *may choose reverse transmit clock, TR_CLK*, which is divided down by circuit 332, as the reference clock REF_CLK for PLL 320. This ensures continued operation if for example, the oscillator producing output 328 or the VCO 334 becomes inoperative or otherwise malfunctions. The multistage multiplexer described may choose one of several inputs for the reference clock used to latch data. Additionally, an upstream or first stage multiplexer having this ability may in fact couple to downstream or second stage multiplexers less capable than the one shown in Fig. 6A:"

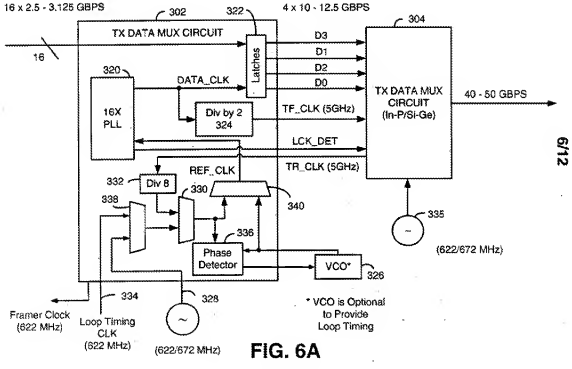


FIG. 6A

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(Specification at page 19, lines 1-9). This capability "ensure[s] continued operation if for example, the oscillator of VCO becomes inoperative or otherwise malfunctions with an alternative source in block 356. (Specification at page 21, *ll.* 4-5).

In kind, Applicant's Independent Claim 1 recites, *inter alia*, a "multistage bit stream multiplexer having a switchable forward/reverse clock relationship comprising: a first multiplexing integrated circuit that receives a first plurality of bit streams at a first bit rate and that produces a second plurality of bit streams at a second bit rate . . . , a second multiplexing integrated circuit that receives the second plurality of bit streams and that outputs at least one high-speed bit stream at a line bit rate that exceeds the second bit rate; and a clock circuit, wherein the clock circuit generates *a forward transmit clock for use by the first multiplexing integrated circuit* in producing the second plurality of bit streams based upon a reference clock signal selectable from a plurality of inputs, *wherein the inputs include a reverse transmit clock generated by the second multiplexing integrated circuit.*" (emphasis added).

Applicant's Independent Claim 14 recites, *inter alia*, an "upstream multiplexing integrated circuit within a multi-stage bit stream multiplexer that operates with a switchable forward/reverse lock relationship with a downstream multiplexing integrated circuit, comprising: a plurality of input ports operable to receive a first plurality of bit streams at a first bit rate; a plurality of output ports to output a second plurality of bit streams at a second bit rate . . . ; and a clock circuit that generates *a forward transmit clock signal for use by the upstream multiplexing integrated circuit* in producing the second plurality of bit streams based upon a reference clock signal selectable from a plurality of inputs, wherein *said inputs include a reverse transmit clock generated by the downstream integrated circuit.*" (emphasis added).

Applicant's Independent Claim 27 recites, *inter alia*, a "method of multiplexing a first plurality of bit streams to at least one high-speed bit stream with a multistage multiplexer, comprising: . . . *multiplexing the first plurality of bit streams* into a second plurality of bit streams at a second bit rate, wherein the second bit rate exceeds the first bit rate; receiving the second plurality of bit streams at a second stage multiplexing integrated circuit at a second bit rate, . . . *multiplexing the second plurality of bit streams* into the at least one high-speed bit stream having a line bit rate that exceeds the second bit rate; and *generating a forward transmit clock from a reference clock signal selectable from a plurality of inputs, wherein the plurality of inputs include a reverse transmit clock generated by the second stage multiplexing integrated circuit.*"

Applicant's Independent Claim 41 recites, *inter alia*, a "method of multiplexing a first plurality of bit streams to at least one high-speed bit stream with a multistage multiplexer, comprises: . . . *multiplexing the first plurality of bit streams* into a second plurality of bit streams

at a second bit rate; . . . multiplexing the second plurality of bit streams into the at least one high-speed bit streams at a line bit rate that exceeds the second bit rate; and generating a forward transmit clock from a reference clock signal selectable from a plurality of inputs, *wherein the plurality of inputs include a reverse transmit clock generated by the second stage multiplexing integrated circuit*." (emphasis added).

Accordingly, Applicant respectfully submits that there has not been a *prima facie* showing that substantiates the rejection of Applicant's claimed invention. There is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the "circuit quality degradation device of Hiramoto and the mono-stage multiplexer device of Graves, which teaches against multi-stage multiplexer devices, to achieve Applicant's claimed invention as set out in Independent Claim 1 and claims 2-5, 9, 11, and 13 that depend directly or indirectly therefrom, as set out in Independent Claim 14 and claims 15-18, 22, 24, and 26 that depend directly or indirectly therefrom, as set out in Independent Claim 27 and claims 29-32and 27 that depend directly or indirectly therefrom, and as set out in Independent Claim 41.

Further, Applicant respectfully submits that the cited references of Hiramoto, Graves and/or Metz *do not* teach or suggest all the claim limitations of Applicant's Claims.

Applicant respectfully requests that these rejections be withdrawn.

2. Allowable Subject Matter

Claims 6-8, 28, 33- 36, and 39-40 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10, 19-21, 23, 25, 37, and 42 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office Action and to include all of the limitations of the base claim and any intervening claims.

Applicant notes with appreciation these indications of allowability.

3. Conclusion

As a result of the foregoing, the Applicant respectfully submits that Claims 1 through 42 in the Application are in condition for allowance, and respectfully requests allowance of such Claims.

If any issues arise, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ksmith@texaspatents.com.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Garlick Harrison & Markison Deposit Account No. 50-2126.

Respectfully submitted,

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